Remarks

Thorough examination by the Examiner is noted and appreciated.

The drawings have been corrected to correct errors noted by Examiner and gratefully acknowledged by Applicants.

The Specification has been corrected to correct errors noted by Examiner and gratefully acknowledged by Applicants.

Claims have been amended and new claims presented to clarify Applicants disclosed and claimed invention.

Support for the amended and newly presented claims is found in the original claims and/or Specification. No new matter has been entered.

For example, support for amended claims 1, 11 and new claim 21 are found in the Specification, at page 19, paragraph 0034 and 0035:

"**Following the first reflow process, the photoresist layer 26 as well as the remaining underlying protective layer 24C is removed** according to a conventional wet chemical striping procedure to leave the solder column 28A as shown in Figure 3B.

According to the present invention, removal of the photoresist layer 16 and the underlying protective layer 24C results in a semiconductor process wafer surface including, for example, **passivation layer 22 surface free of photoresist residue**. As such, the **subsequent second reflow processes to form solder ball 28B as shown in Figure 3C are accomplished without adverse affect from residual photoresist** and while ensuring that subsequent semiconductor packaging steps likewise proceed without adverse consequences from residual photoresist remaining on the process wafer surface thereby increasing a throughput and semiconductor wafer package yield"

New claims 22 and 23 find support in the Specification, for example, at page 19, paragraph 0031:

"**Prior to stencil printing the solder paste, the protective layer 24C and first photoresist layer 24B within opening 28 are removed according to a conventional ashing process**, for example an oxygen containing reactive ion etching process, to give the structure shown in Figure 2F."

Support for new claim 24 is found, for example, at page 15, paragraph 0027:

"After the chip bonding pad 20 is formed, a passivation layer 22 of, for example, silicon nitride (SiN), or silicon dioxide (SiO_2) is formed over the semiconductor device surface excluding a portion overlying the chip bonding pad 20"

Claim Rejections under 35 USC 103(a)

1. Claims 1-20 stand rejected under 35 USC 103(a) as being unpatentable over Costas et al. (U.S. Patent 6,137,125) in view of admitted prior art and further in view of Lee (US U.S. Patent 6,410,414)

Costas et al. disclose a 2-layer hermetic coating for on wafer encapsulation of GaAs monolithic microwave integrated circuits (MMIC) using benzocyclobutene (BCB) and ceramic materials for the coating to provide both mechanical protection and protection from moisture to the MMIC (see Abstract; col 2, lines 21-30). Costas et al. teach the benefit of using BCB in the hermetic coating includes its low diel3ctric constant useful for capacitive decoupling of an underlying MMIC (see col 2, lines 33-44). Costas et al. disclose a method where a BCB layer is first formed followed by forming an overlying ceramic layer, followed by forming a photoresist over the ceramic layer followed by patterning and RIE etching to expose bonding pads (see col 1, lines 47-67).

Examiner argues that the disclosure of Costas et al. is "equivalent to forming of solder columns through a patterned resist stencil either (1) of photosensitive BCB or (2) with

underlying non-photosensitive BCB, which has been patterned through the resist stencil."

Costas et al. is non-analogous art. However, even assuming that Costas et al. is analogous art, the disclosure of Costas et al. is inconsistent with the principal of operation of Applicants disclosed and claimed invention and does not recognize the problem that Applicants invention has recognized and solved.

Costas et al. does not disclose or teach a solder ball or solder column forming process as disclosed and claimed by Applicants. Costas et al. does not disclose a BCB containing material that has a glass transition temperature greater than 300 °C or 350 °C. Significantly Costas et al. does not disclose forming a patterned photoresist layer over (on) the protective layer of Applicants followed by subjecting both the photoresist and protective layer (e.g., BCB) to a solder reflow temperature.

The use of a BCB layer in the manner disclosed by Costas et al. neither recognizes nor solves the problem that Applicants have recognized,disclosed, claimed, and solved; " a method for protecting a semiconductor process wafer surface from contacting thermally degraded photoresist to improve a solder ball formation process"

In addition to failing to disclose **any** of the elements of Applicants claimed invention except a "semiconductor process wafer", Costas et al. would defeat the purpose and operation of Applicants claimed invention.

Examiner cites Applicants for admitted prior art put forth in the background of the invention to outline the problem presented and solved by Applicants claimed invention. Examiner improperly attempts to find motivation for making Applicants claimed invention in Applicants disclosure. There is no motivation for combining Costas et al. with Applicants admitted prior art other than Applicants disclosure.

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's**

disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Lee discloses a process whereby a BCB layer having a low water intake rate and an excellent blocking effect against alpha particles is formed between an alpha particle source such as a solder ball and sensitive integrated circuit devices.

Lee does not help Examiner in establishing a *prima facie* case of obviousness with respect to Applicants claimed invention. There is no apparent motive form combining Costas et al. and Lee **(other than Applicants disclosure)** as they deal with entirely different processes and use a BCB layer for entirely different purposes. However, even assuming *arguendo* a proper motive for combination, such combination does not disclose, teach, or suggest Applicants disclosed and claimed invention. Lee does not disclose a solder ball formation process. Lee does not disclose exposing a photoresist layer in contact with an underlying protective layer (e.g., BCB) at a solder reflow temperature. Moreover, Lee does not disclose **removing** the BCB layer prior to a solder ball forming reflow temperature (see e.g., claim 11, and new claim 21), destroying the principal of operation of Applicants disclosed and claimed invention and eliminating the

stated motives for using the BCB layer (left in place) taught in both Costas et al and Lee.

The fact that Lee discloses a BCB layer that has a glass transition temperature of 350 °C is not sufficient to make Applicants disclosed and claimed invention *prima facie* obvious.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).*

Applicants respectfully suggest that Examiner has impermissibly attempted to engage in hindsight reasoning to recreate Applicants invention using Applicants disclosure as a roadmap. Nevertheless, Examiner has failed to produce Applicants claimed invention.

Neither Costas et al. nor Lee, in view of the problem in the prior art disclosed by Applicants which is Applicants have solved by their disclosed and claimed invention, are sufficient to make out a *prima facie* case of obviousness with respect to Applicants

amended independent claims, and are therefore insufficient with respect to the dependent claims.

The claims have been amended and new claims added to clarify Applicants invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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